Controlling the Data Path Acceleration Behaviors using ForCES

draft-cao-dataplane-acceleration-framework-01

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The Matter of Fact

- CAGR of Global Internet Traffic is 24% *
 - Fixed CAGR = 21%
 - Mobile CAGR = 68%
- Chipset performance CAGR is around 14%
- The '*Forwarding Gap*' is therefore formed



* Cisco Visual Networking Index: Forecast and Methodology, 2012–2017

Current practice to cover the 'Forwarding Gap'

- Data Plane Acceleration
 - Data Plane Develop Kit, i.e. DPDK
 - Accelerated virtual switch
 - Open Data Plane project (www.opendataplane.org)
- Tricks essentially it is to create '*Fast Paths*'
 - Efficient Run-time Memory Allocation, e.g., no malloc
 - Minimize Data Copies in Memory
 - Align data structures for best cache usage
 - Have data at the right place at the right time

Fast Path across devices



- The higher layer the packet is being processed, the more challenge to its performance
- For some L4-7 network functions, the NF can establish the session and offload the traffic to the L2-3 infrastructure.
- Information (meta-data) conveyed from the NFs to forwarding devices

Current DPA Architecture



What's missing?

- DPDK considers the data as a single block, not able to differentiate flows
 - Some flows are not necessarily accelerated
 - Some flows are more important than others
 - Different users have different requirements
- In any case, the data plane need to be informed about such information

Relationships to ForCES



- FE elements to CE
 - Notification of DPA capabilities
 - Notification of the flow identification
 - Notification of chipset information, already there?
- CE elements to FE
 - Configure the FE w.r.t. its DPA behaviors
 - Configure flow priorities on the FE

Virtualization or not ?





CE

FE

Next Steps?

Submit a new forces scenario and possibly a solution draft in forces

• Consider this a work group direction?